nxTCP

Standard Edition

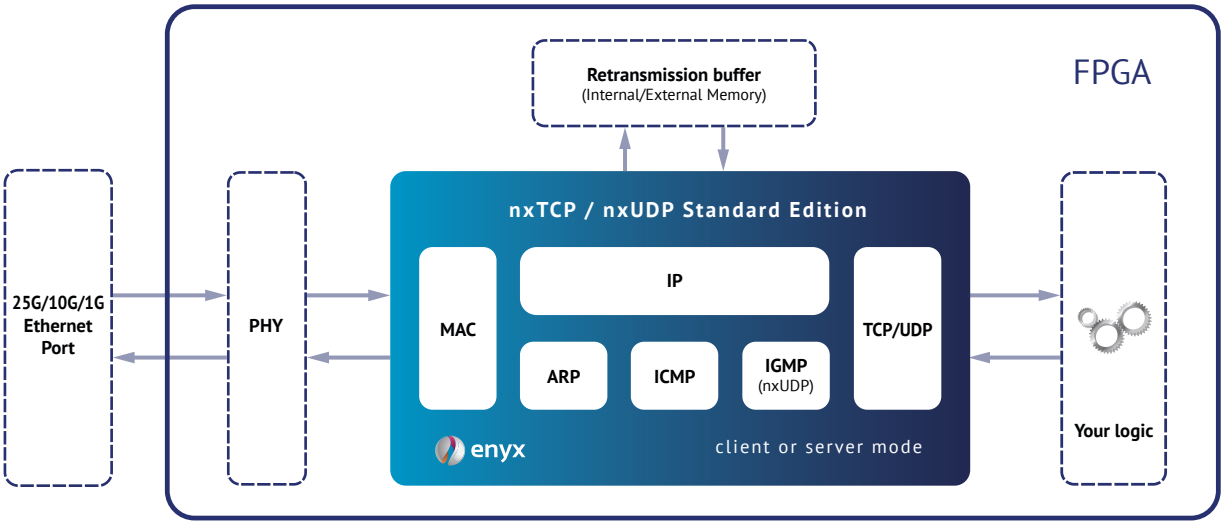
25G/10G/1G
TCP/IP + MAC
IP Core for FPGAs

nxUDP

Standard Edition

25G/10G/1G
UDP/IP + MAC
IP Core for FPGAs

hardware acceleration experts



available on

compliant with

The world's most reliable and mature full hardware TCP, UDP and MAC IP Cores.

Bring the best-in-class network connectivity to your hardware design with Enyx rock-solid and acclaimed Ethernet IP Cores. Minimize time-to-market with our full RTL implementation and support. Stay always at the forefront of technology with our frequent updates with the latest improvements and optimizations.

Client profiles include

- High performance computing
- Military & defense
- Universities & research Labs
- Technology manufacturers
- Telecom operators
- Aerospace & aeronautics

Key points

25G/10G/1G Ethernet connectivity. Maximum bandwidth delivered with low latency.

Full RTL Layers 2, 3 and 4, which include Enyx proprietary full-hardware TCP/IP and UDP/IP, ARP, ICMP, IGMP and MAC implementations.

Easy to use standardized Avalon and AXI-4 interfaces.

Support multiple instances per FPGA and multiple logical interfaces per instance, each of them with a unique IPv4, MAC address, VLAN ID, Gateway and Mask.

Up to to 4096 (TCP) and 256 (UDP) simultaneous sessions per instance, each of them configurable dynamically in server or client mode.

Support for UDP Unicast and Multicast transmit/receive

Supported platforms

ALTERA now part of Intel

XILINX

Arria 10 FPGA • SoC

Stratix V FPGA

Stratix 10 FPGA • SoC

KINTEX 7 UltraSCALE UltraSCALE+

VIRTEX 7 UltraSCALE UltraSCALE+

ZYNQ

Available reference designs

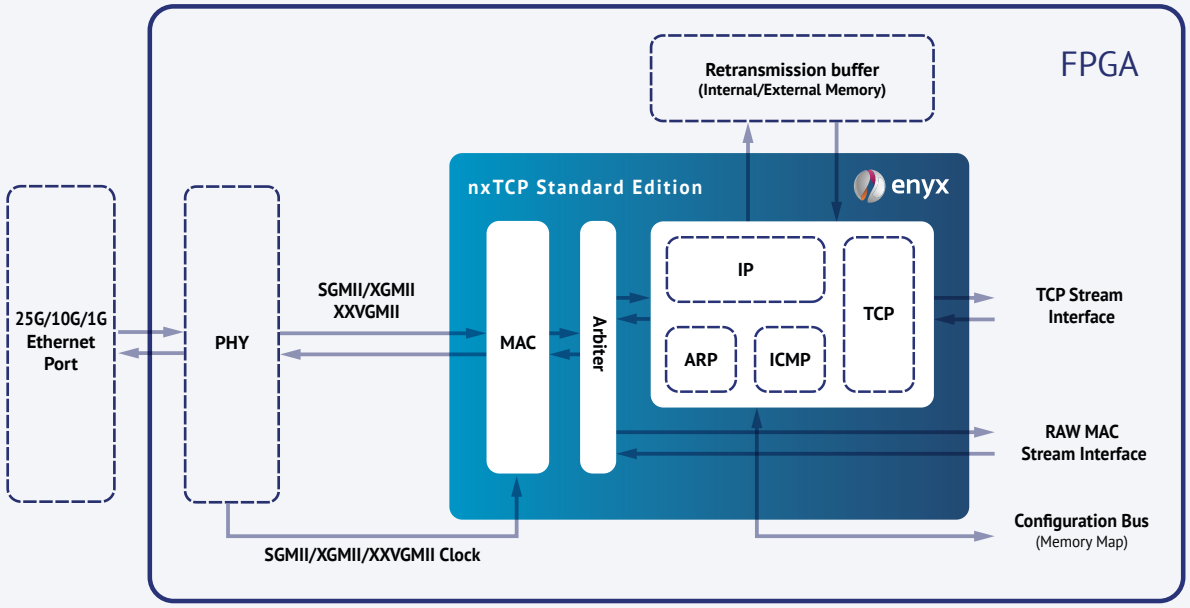
- Altera Stratix V GX FPGA Development Kit
- BittWare S5-PCIe-HQ
- BittWare XUPP3R
- ReFLEX CES XpressGXA10-LP1150
- ReFLEX CES XpressGX5-LP QE, SE, HE
- ReFLEX CES XpressGX4-LP
- ReFLEX CES XpressV7-LP HE
- ReFLEX CES Attila Instant-DevKit Arria 10 FPGA FMC IDK
- Xilinx Kintex-7 FPGA KC705 Evaluation Kit
- Xilinx Virtex-7 FPGA VC707 Evaluation Kit
- Xilinx Virtex-7 FPGA VC709 Connectivity Kit
- Xilinx Zynq-7000 All Programmable SoC ZC706 Evaluation Kit

Enyx Certified Board partners

ReFLEX CES Custom Embedded Systems

BittWare FPGA PLATFORMS

Technical specifications



nxTCP Standard Edition diagram

Management of layers 1, 2, 3 and 4 (OSI Model), compliant with
- Layer 1: IEEE802.3
- Layer 2: IEEE802.3, ARP (Address Resolution Protocol)
- Layer 3: IPv4 and ICMP (Internet Control Message Protocol)
- Layer 4: TCP (RFC 793) or UDP

Session management
- Up to 4096 (TCP) and 256 (UDP) simultaneous sessions
- Client or server mode configurable at runtime

User Configurable TCP Options
- VLAN Priority, with insertion of PCP and DEI fields at emission
- MSS
- Window Scale Factor
- Timestamp

Customizable MTU (Maximum Transmission Unit)
- Up to 9000 bytes payload to support from standard to jumbo frames

MAC in Promiscuous mode (transparent)

Access to RAW MAC Stream Interface:
- **1G**: 64-bit @ 125 MHz
- **10G**: 64-bit @ 156.25 MHz
- **25G**: 128-bit @ 195.3125 MHz

ICMP and ARP protocols

IGMP v2 protocol
- Support for IGMP v2 Membership Report/Leave message generation (for UDP
- Support for IGMP v2 Membership Query message reception. The UDP stack will multicast groups) reply to a Query message if necessary.

Supports Unicast and Multicast transmit/receive

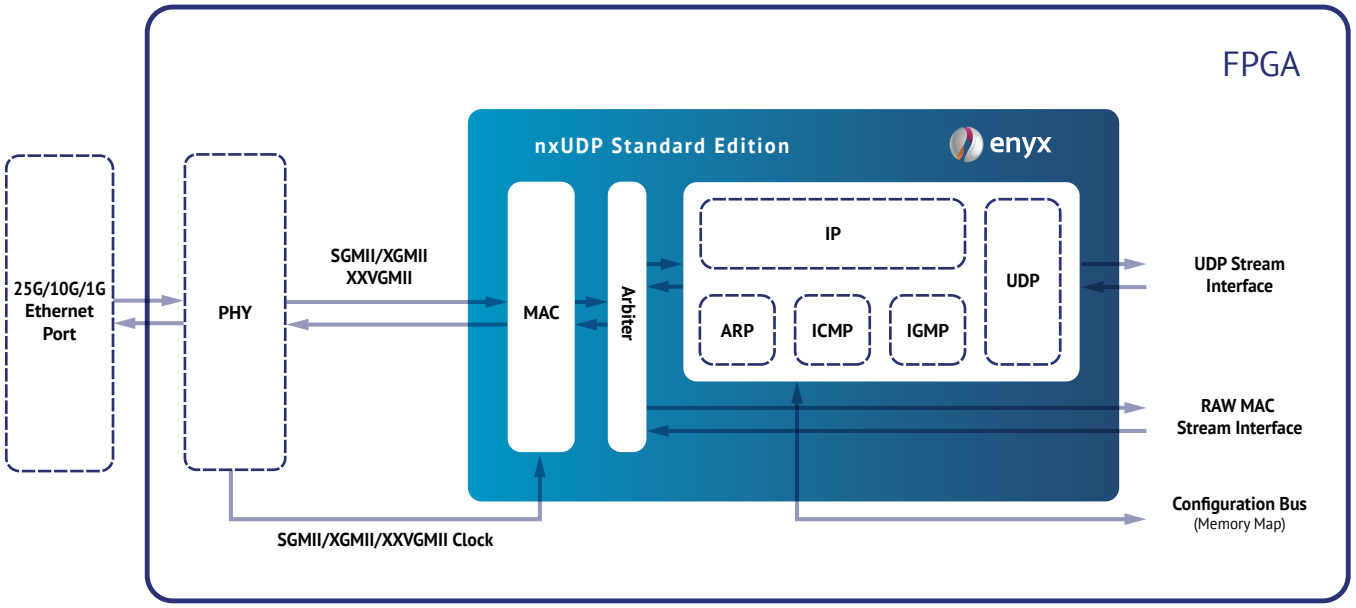
Multiple Interface
- Up to 8 logical interfaces per instance
- Linked to any session
- VLAN configurable per interface

Avalon/AXI-4 Streaming
- 128-bit wide interface running at 125 MHz (1G), 156.25 MHz (10G), 195.3125 MHz (25G) for TCP/UDP client port

IP configuration/management
- 32-bit Avalon-MM/AXI- 4 lite slave control interface for MAC and TCP/UDP
- Status and statistics available for monitoring at MAC or TCP/UDP session level

Customizable TCP retransmission buffer
- Customizable buffer size (depth and width)
- Customizable Internal or External memory support (DDRx, QDRx, ...) depending configuration on performance and FPGA size requirements

PHY Interface
1G - 10/100/1000M - 1000BASE-X/SGMII interface (9-bit @ 125 MHz) to integrated SGMII PHY or 1000BASE-X with PMA-PCS
10G - XGMII interface (72-bit @ 156.25 MHz) to integrated XAUI PHY or 10GBase-R with PMA-PCS
25G - XXVGMII interface (72-bit @ 390.625 MHz) to integrated XXVAUI or 25GBase-R with PMA-PCS



nxUDP Standard Edition diagram

Enyx IP Cores compared

	nxTCP & nxUDP Standard Edition	nxTCP Financial Edition	nxPCS + nxMAC Financial Edition
Latency	Very low	**Ultra low**	
Target audience	Most industries	High Perfomance Traders	
Deliverables			
Layer 1 (PCS)		✓	✓
Layer 2 (MAC)	✓	✓	✓
Layer 3 (IP)	✓	✓	
Layer 4 (TCP/UDP)	✓	✓	
Supported Sessions	Up to 4096 (TCP) and 256 (UDP)	1 to 128	-
Connectivity			
1G	✓		
10G	✓	✓	
25G	✓		
Supported FPGAs			
Altera Stratix 4	✓		
Altera Stratix 5	✓	✓	
Altera Stratix 10	To be supported	To be supported	
Altera Arria 10	✓	✓	
Xilinx Kintex/Virtex-7	✓		
Xilinx Kintex/Virtex UltraScale	✓		
Xilinx Kintex/Virtex UltraScale+	✓	✓	
Xilinx Zynq-7000	✓		

Package contents

IP Core
- Libraries for functional simulation
 Synthesizable VHDL and Verilog RTL (encrypted) for synthesis/implementation

Testbench
- Simulation libraries

Client-Server Reference Designs
- Simulation environment and scripts
- Quartus II and Vivado Synthesis/implementation project for supported partner's boards

Complete Documentation
- User's manual
- Getting started guide

Technical Support and Maintenance Updates
- 1 year of technical support
- 1 year of IP updates

Contact us

contact@enyx.com

Sales Contact : **contact@enyx.com**
Media Contact : **communication@enyx.com**

Europe **+33 1 4523 1349**
America **+1 347 201 4827**
Asia **+852 5808 5363**

North American Offices

1440 Broadway
Suite 2332
New York, NY 10018
UNITED STATES

350 N Orleans Street
Suite 9000N
Chicago, IL 60654
UNITED STATES

European Office

8 Rue Greneta
75003 Paris
FRANCE

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